WHAT IS CLAIMED IS:

1. A memory comprising:

a counter configured to increment and store an address data pointing to a first array address with each transition of a clock signal;

a comparator configured to compare the first array address with a second array address read out during a first cycle, said comparator further configured to assert a first signal if the first array address matches the second array address or if the first array address matches an address of a neighboring array of the second array address; and

a first circuit configured to generate a refresh array address during a second cycle immediately succeeding the first cycle, wherein the first circuit generates a refresh array address that is different from the second array address or the address of the neighboring array of the second array address.

2. The memory of claim 1 further comprising:

a pipelined shift register having at least two pipeline stages, wherein with each transition of the clock signal, the data stored in the counter prior to the increment is shifted and loaded into the first stage of the pipeline, and a previous data stored in the first stage of the pipeline is shifted and loaded into the second stage of the pipeline.

3 . The memory of claim 2 further comprising:

a multiplexer configured to receive the data stored in the counter and the second stage of the pipeline at its respective first and second input terminals.

4. The memory of claim 3 wherein said multiplexer receives the first signal generated by the comparator at its select input terminal.

5. The memory of claim 4 wherein the memory is a DRAM-based SRAM.

6. The memory of claim 5 further comprising:

a plurality of sense amplifiers that are shared by each pair of neighboring arrays.

7. The memory of claim 5 wherein each array includes a plurality of memory cells disposed along rows and columns of that array.

8. A method for operating a memory device comprising:

selecting a first array to perform a read operation during a first operation cycle; and

selecting a second array to perform a refresh operation during a second operation cycle immediately succeeding the first operation cycle, wherein the second array is different from both the first array and a neighboring of the first array.

9. The method of claim 8 further comprising:

comparing an address of the first array with a third array address; and

asserting a signal if the third array address matches the first array address or an address of its neighboring array.

10. The method of claim 9 further comprising:

setting an address of the second array equal to the third array address if the signal is not asserted.

11. The method of claim 10 further comprising:

storing each of the first, second and third array addresses.

12. The method of claim 11 further comprising:

incrementing the second array address; and

shifting the said second array address before it is incremented.

13. The method of claim 12 wherein the first and second array addresses differ by a count of two addresses.

14. The method of claim 13 wherein the memory is a DRAM-based SRAM memory.